SPICE up the development of a step recovery diode frequency multiplier

With the aid of one of the many versions of SPICE, the design of frequency multipliers using step recovery diodes is expedited and made more tractable.

By George H. Stauffer Jr.

The step recovery diode (SRD) operates in one of two states. The state is determined by the presence or absence of the stored charge at the PN junction. When a charge is present, the equivalent circuit of the diode is a large valued diffusion capacitance in parallel with the AC resistance of the forward biased diode. This combination is a good approximation of a short circuit. The amount of charge stored at the junction is determined by the forward current I_F, the time it flows t_F, and the carrier lifetime according to

$$Q = I_F \cdot \tau \cdot \left(1 - e^{-\frac{t_F}{\tau}}\right) \quad (1)$$

If all of the charge is removed by a reverse current I_R, then the diode changes almost instantaneously to its second state. In this high-impedance state, the diode looks like a small capacitor whose value is equal to the depletion layer capacitance of the junction. If a forward current flows for a time >> τ and then a reverse current I_R begins, then the time t_s that elapses before all the charge is removed and the diode changes to its high impedance state is

$$t_s = \tau \cdot \ln\left(1 + \frac{I_F}{I_R}\right) \quad (2)$$

A common way to measure the carrier lifetime τ is to set I_F/I_R equal to 1.718 so that the time elapsed from when the reverse current begins, to when the diode turns off, is equal to the carrier lifetime. To minimize input losses caused by carrier recombination, the selected diode should have a carrier lifetime of $\tau \ddagger 5/w_{in}$. For a 100 MHz input, the diode should have $\tau \ddagger 8$ ns.

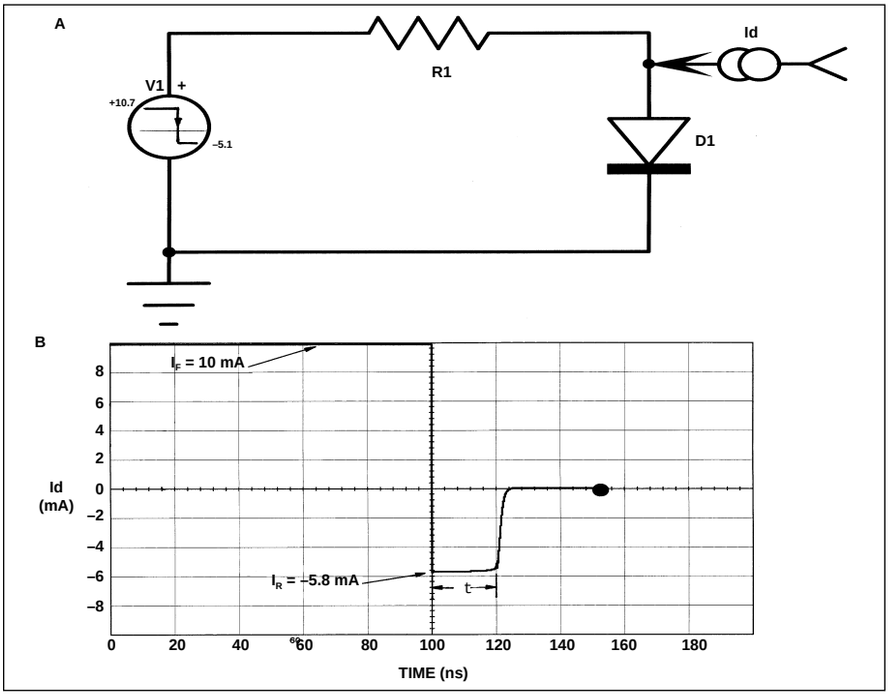


Figure 1. Testing SPICE model for SRD behavior. (a) Test circuit (b) Diode current showing sudden transistion after τ seconds.

SPICE model of SRD

Before proceeding with the design, it is important to confirm that the generic SPICE model for a PN junction diode will exhibit a charge-controlled step change in impedance. Figure 1a shows a simple SPICE circuit that tests for SRD action using I_F = 10 mA and I_R = 5.82 mA, a ratio of 1.718. The model parameters of primary importance for SRD modeling are carrier lifetime τ (TT), depletion layer capacitance at a specified value of reverse voltage C_{j-6} and junction-grading coefficient M. The first two parameters are supplied by the manufacturer. The grading coefficient determines the variation of depletion capacitance with reverse voltage. A value of M = 0.5, typical for an abrupt junction diode, was chosen and provided good results in the simulation. The SPICE model requires the value of depletion capacitance at zero volts C_{j0}. This may be calculated from the equation for depletion layer capacitance shown in Equation 3

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_j}{\phi}\right)^M} \quad (3)$$

V_j is the reverse junction voltage and ϕ is the contact potential, which is set equal to 0.6 V.

Breakdown voltage and series resistance play a secondary role of limiting the maximum power available from the multiplier circuit. The model parameters used for the SRD are shown in Table 1.

The results from the test circuit are shown in Figure 1b and demonstrate the effect of charge storage. Because I_F/I_R =1.718, the charge removal time t_s is equal to τ The voltage source goes

Parameter	Symbol	Value
Reverse saturation current	I_s	1 nA
Cj at –6 V	C_{j-6}	0.7 pF
Cj at 0 V	C_{j0}	2.3 pF
Carrier lifetime	TT	20 nS
Breakdown voltage	BV	–15 V
Series resistance	R_s	0.7 W
Emission factor	N	1.5
Grading coefficient	M	0.5

Table 1. SRD SPICE model parameters.

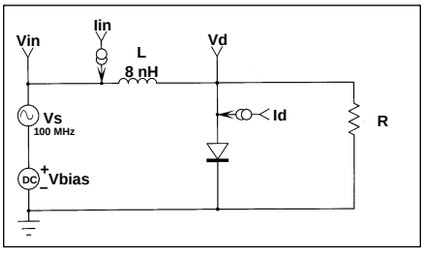


Figure 3. Basic multiplier with calculated component values ready for SPICE simulation.

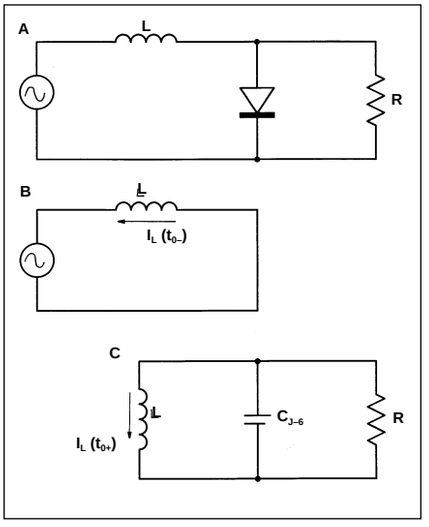


Figure 2. Two states of the basic multiplier circuit. (a) Basic circuit. (b) Circuit with SRD in low impedance state at t_{0-} (c) Circuit with SRD in high impedance state at t_{0+}.

negative at t = 100 ns, but because of the stored charge, the diode continues to conduct a negative current for 20 ns. The transition time from on to off is caused by the RC time constant of the 1 kW resistor and the diode depletion layer capacitance.

Initial design of 100 MHz multiplier

Initial circuit values are found using the simplified multiplier circuit shown in Figure 2a. During the positive portion of the input voltage, and for part of the negative portion, the equivalent circuit is shown in Figure 2b where the diode is represented by a short circuit. Here, the circuit is shown at t0- the instant before the diode switches to its high impedance state. A large reverse current that has been removing charge from the SRD is flowing through the inductor and is about to undergo a large di/dt when the diode switches at $t = t_0$. Figure 2c shows the circuit at $t = t_{0+}$. This is a simple parallel inductive-capacitive-resistive (LCR) circuit with an unloaded resonant frequency $w_r @ 1/\sqrt{LC_{j-6}}$ and $Q = R/w_rL$.

A large amplitude negative pulse begins at $t = t_{0+}$. The pulse width is approximately one half the period of the resonant frequency of the parallel LC circuit. More accurate design formulas are available [2, 3 and 4]; however, significant design time is saved by using these approximate methods and then using the SPICE simulation to arrive at the final values.

The initial value for the series inductance L is calculated by considering the required pulse width. Power at the output frequency f_o is maximized for pulse widths between $1/2f_o$ and $1/f_o$. For f_o = 3.2 GHz, a pulse width of 234 ps is halfway between $1/2f_o$ and $1/f_o$. For this pulse width, the resonant frequency of the parallel LC circuit of Figure 2c is f_r = 2.17 GHz. A value of Q @ 1 is recommended for stable operation. For f_r = 2.17 GHz and C_{j-6} = 0.7 pF, a value of L = 8 nH is calculated using $w_r @ 1/\sqrt{LC_{j-6}}$ and R=107 W is found using $Q = R/w_rL = 1$.

SPICE simulation of multiplier circuit

The simplified multiplier circuit using the initial values is shown in Figure 3. Voltage source V_s supplies a 100 MHz sine wave with 600 mV peak amplitude. Voltage source V_{bias} is a DC bias voltage. This bias voltage is adjusted so that the current flowing through the inductor is at its negative peak ($dI_L/dt = 0$) when the diode switches to the high impedance state. Figures 4a, b and c show the results of the SPICE simulation. Note that the diode current is at its peak maximum value at the transition time. The output pulse has a width @ 260 ps and an amplitude slightly less than the diode

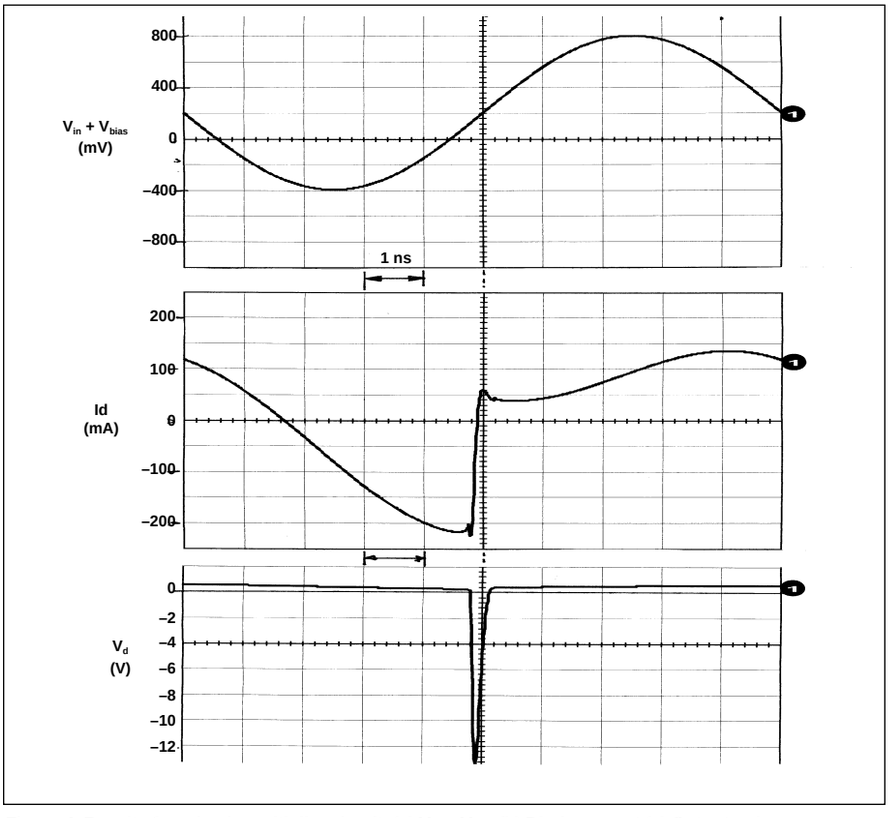


Figure 4. Results from basic multiplier circuit. (a) V_{in} + V_{bias} (b) Diode current (c) Output pulse.

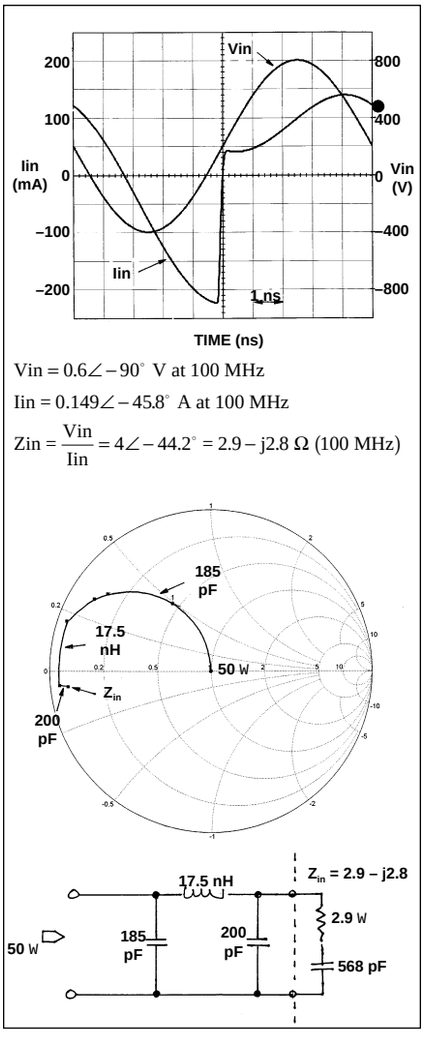


Figure 5. Input impedance Z_{in} at 100 MHz. (a) input voltage, current waveforms and calculation of Z_{in}. (b) Matching to Zin with p network.

breakdown voltage.

Input match at 100 MHz

The actual circuit will be driven by a 100 MHz generator with a 50 W source impedance. For best efficiency, it is necessary to match the relatively low impedance of the SRD circuit to 50 W at the input frequency. The ratio of the Fourier components of the input voltage, and current at 100 MHz is the impedance of the diode under operating conditions. A fast Fourier transform (FFT) post-processing feature available in many versions of SPICE can be used for this purpose. Figure 5a shows the input current and voltage waveforms from the circuit of Figure 3 and the calculation of Z_{in}. Figure 5b shows Z_{in} plotted on a Smith chart and the results after matching with an LC p network.

	Pin	Vbias	Harmonic :	3.1 GHz	3.2 GHz	3.3 GHz
SPICE	14.5 dBm	+ 0.3 V		–12.3 dBm	–9.1 dBm	–15.2 dBm
Measured	14.5 dBm	+ 0.3 V		–18 dBm	–10.3 dBm	–13 dBm

Table 2. SPICE vs. measured results.

Ringer circuit

A quarter wave resonant transmission line at 3.2 GHz is one way to boost the level of the desired harmonic above the other harmonics before additional filtering. The line is terminated with a resistance chosen so that the loaded Q of the resonant line is approximately (p/4)N, where N is the ratio of desired output frequency to input frequency (N = 32 for this design). The output of the resonant line for this value of Q is a damped sine wave that spans one input cycle. Q is adjusted by varying the degree of coupling to the 50 W load with a small series capacitor. The length of line is adjusted so that the sinusoid rings with a period of 312 ps. The characteristic impedance Z_0 of the line is made equal to the shunt resistance R in Figure 3. Z_0 is 107 W for this design, and is the resistance that the pulse sees before the first reflection arrives back at the SRD. Figures 6a, b and c show the final circuit, the damped waveform and an FFT of the damped waveform. The power in the 3.2 GHz line is –9.1 dBm with 14.5 dBm input.

Results from working circuit

The layout of the 100 MHz to 3.2 GHz multiplier is shown in Figure 7. The circuit was built on a 2† · 2† FR-4 board, 0.031†thick using 0805 and 0603 surface mounted components. Comparison between simulated and measured performance is shown in Table 2.

Conclusion

The simple SPICE model of a 100 MHz to 3.2 GHz multiplier predicted actual circuit operation accurately for an output frequency in the low microwave range using the generic SPICE models for the SRD and all passive components. The extremely non-linear behavior of an SRD diode is easily handled by the time-

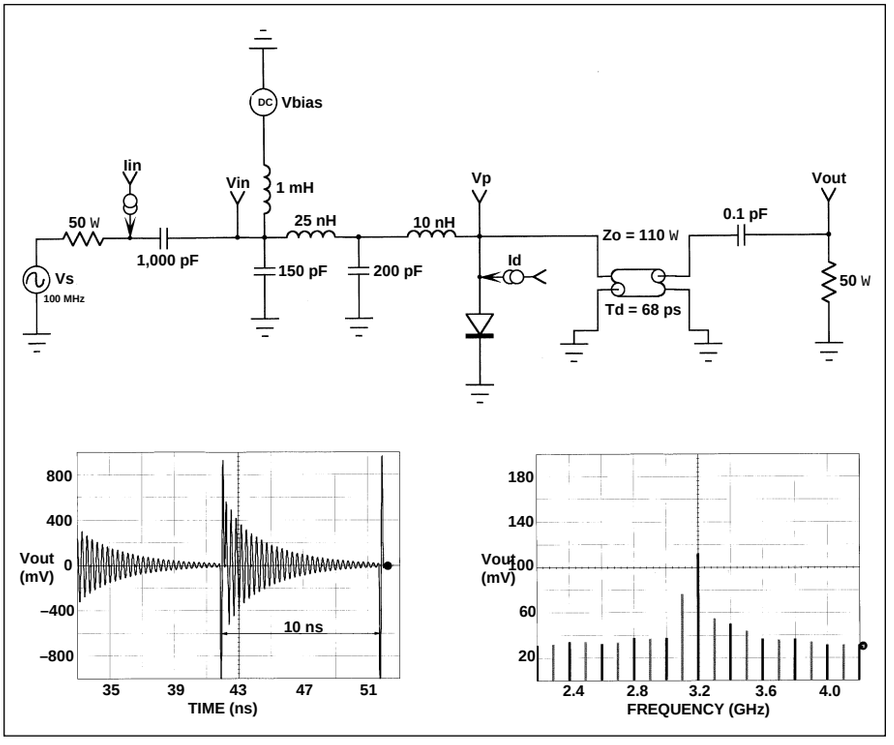
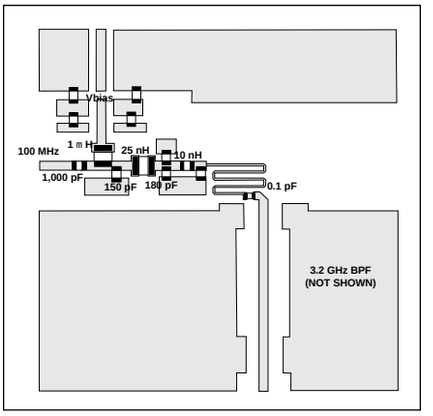


Figure 6. Final multiplier circuit (a) Circuit with input match and ringer. (b) Damped waveform at output. (c) Output spectrum.



domain simulator resulting in short simulation times. Adjustments to the circuit model are reflected in circuit performance that reduces time spent doing detailed theoretical calculations and hardware iterations. RF

References

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About the author

George H. Stauffer Jr. is an assistant professor of electronics and electrical engineering at Capitol College, Laurel, MD. Previously he worked as an RF and microwave circuit design engineer in the Radio Receiver Group of Watkins Johnson Company in Gaithersburg, MD. He holds the A.B and B.S.E.E degrees from Lafayette College, Easton, PA. and an M.S. degree from The Johns Hopkins University. He can be reached at 301-369-2800 or by e-mail at *gstauffer@capitol-college.edu*.